IN THE CLAIMS:

Claim 2 was previously canceled. No claims have been amended herein. All of the pending claims 1 and 3 through 15 are presented below. This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (previously presented) A substrate for testing at least one semiconductor device having at least one substantially spherical interconnection element protruding from a surface thereof, consisting essentially of:

a semiconductor substrate having a dielectric layer on an exposed surface thereof;

at least one conductive trace over the dielectric layer;

a passivation layer over the at least one conductive trace and the dielectric layer; and

a metal-lined via extending through the passivation layer to a portion of the at least one conductive trace, wherein the metal of the metal-lined via is in electrical communication with the at least one conductive trace, wherein the metal-lined via is sized and configured to receive, without deformation, the at least one substantially spherical interconnection element protruding from the at least one semiconductor device to a depth corresponding to approximately 10% to 50% of an overall height of the substantially spherical interconnection element and establish an electrical connection therewith at the depth by way of biased contact of only a portion of an interior surface of the metal-lined via with only a portion of an exterior surface of the substantially spherical interconnection element received therewithin.

2. (canceled).

3. (previously presented) The substrate of claim1, wherein the metal-lined via is formed of a size and shape to receive approximately 30% of the overall height of the substantially spherical interconnection element.

4. (previously presented) The substrate of claim 1, wherein the metal-lined via includes sloped sidewalls.

5. (previously presented) The substrate of claim 1, wherein the metal-lined via includes stepped sidewalls.

6. (previously presented) The substrate of claim 1, wherein the at least one conductive trace comprises copper.

7. (previously presented) The substrate of claim 1, wherein the passivation layer comprises polyimide.

8. (previously presented) The substrate of claim 1, wherein the metal-lined via comprises a metal from the group comprising gold, platinum, palladium, and tungsten.

9. (previously presented) The substrate of claim 1, wherein the dielectric layer comprises silicon dioxide.

10. (previously presented) The substrate of claim 1, wherein the passivation layer has a thickness of about 20 to 25 microns.

11. (previously presented) The substrate of claim 1, wherein the passivation layer has a thickness of about 100 microns.

12. (previously presented) The substrate of claim 1, further comprising:
at least one additional conductive trace over the passivation layer;
a second passivation layer over the at least one additional conductive trace; and
a second metal-lined via in the second passivation layer in electrical communication with the at least one additional conductive trace.

13. (previously presented) The substrate of claim 1, wherein the metal-lined via is sized and configured to establish the electrical connection only along at least one contact line consisting of the portion of the interior surface of the metal-lined via at least partially circling the portion of the exterior surface of the substantially spherical interconnection element.

14. (previously presented) The substrate of claim 1, wherein the metal-lined via is sized and configured to establish the electrical connection only along a plurality of contact lines consisting of the portion of the interior surface of the metal-lined via at least partially circling the portion of the exterior surface of the substantially spherical interconnection element.

15. (previously presented) The substrate of claim 14, wherein the plurality of contact lines at least partially circling comprise a plurality of contact lines circling.